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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,416	10/23/2003	Anthony Gus Aipperspach	AUS920030577US1	8492

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EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,416	AIPPERSPACH ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-19* is/are allowed.

6)☒ Claim(s) *1-9,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/22/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Finite state machine 110 should be changed to 115 to be consistent with the specification of page 6, line 22.

Rising and falling edge detector 115 should be changed to 120 to be consistent with the specification on page 5, line 27.

Monostable trigger 120 should be changed to 125 to be consistent with the specification on page 6, line 28.

Irregular clock input 105 should be changed to 110 to be consistent with the specification on page 6, line 22.

Inverter 125 should be changed to 135 to be consistent with the specification on page 7, lines 5 and 13.

Operational amplifier 135 should be changed to 130 to be consistent with the specification on page 7, lines 5, 6 and 13.

Integrating circuit 130 should be changed to 140 to be consistent with the specification on page 7, line 12.

Claim Objections

2. Claims 2, 7 and 11 are objected to because of the following informalities:

With respect to claim 2, line 2 the recitation of the clock input "coupled to the source" should be changed to -- coupled to the drain-- because the unconditioned clock input is coupled to the drain of the p-type FET.

With respect to claim 2, line 2 the recitation of "a positive FET" on line 2 should be changed to --a P-type FET-- because it is incorrect to recite a FET being positive or negative.

With respect to claim 7, line 3 "and clock pulse inverter" should be changed to --and a clock pulse inverter--.

With respect to claim 11, line 1 "The method of claim 11" should be changed to --The method of claim 10--. For purposes of the examination it is assumed claim 11 depends on claim 10. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 1, 3, 6, 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, line 12 it is unclear to what the applicant means by the "conditioned clock signal output" because only elements have outputs i.e. a clock signal cannot have an output.

With respect to claim 3, it is unclear what unit comprises the leak detector because in figure 4 the leak detector (145) is outside of the correction block 140.

With respect to claim 6, it is unclear which is the conditioned clock pulse because according to claim 1 (on which this claim depends) the conditioned clock pulse is not between the delay sub-block and the correction block but between the HI/LO shuttle clock and the correction block.

With respect to claim 20 and 21, it is unclear as to how the claim reads on the recited invention because no code to implement this hardware is apparent in the disclosure.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sher (US 2001/0011913).

With respect to claim 1, figure 2 of Sher discloses a pulse width limiting circuit, comprising: a clock signal correction block (3, 5,7, 9 and 27) configured to receive a conditioned clock pulse (XCLK) and generate a corrected clock output signal (at node D), wherein the clock signal comprises a train of clock pulses, each of which has a rising clock edge, a falling clock edge and a variable width; a block delay module (21, 23 and 25) configured to accept an unconditioned clock signal (CLKY) and introduce a specified pulse width delay, wherein the block delay module comprises a plurality of delay sub-blocks of fixed delay; and a high low clock pulse shuttle circuit (elements of 11) configured to accept the conditioned clock signal output (at node D), but fails to disclose the high low clock pulse shuttle comprising a first field effect transistor (FET)

coupled to the correction block and a second FET coupled to a conditioned clock signal interconnect. "DIGITALINTEGRATED CIRCUITS –A Design Perspective", Jan M. Rabaey, Prentice Hall (1996) Chapter 4, page 193 teaches the internal elements of a two input NAND gate using CMOS technology. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use combinational FETs to make the NAND gate of Sher for the well known purpose of minimizing power consumption.

With respect to claim 2, the resulting combination above produces a circuit wherein the unconditioned clock input is coupled to the drain of a p-type FET in the high low clock pulse shuttle (p-type FET's of 11).

With respect to claim 3, the resulting combination above produces a circuit where a correction block circuit further comprises a correction unit (5, 7, 9 and 27) and a leak detector unit (3), wherein the correction block is employed to transmit the clock pulse to the high low clock pulse shuttle (p-type FETs of 11).

With respect to claim 4, the resulting combination above produces a circuit wherein the high low clock pulse shuttle (p-type FETs of 11) is coupled to an interconnect (wire between 11 and 13), wherein the interconnect is employed to convey an unmodified clock pulse.

With respect to claim 5, the resulting combination above produces a circuit further comprising a node (going into 21) to transmit the clock pulse between stages of a delay sub-block (21, 23 and 25).

With respect to claim 6, the resulting combination above produces a circuit,

further comprising a node (at C) to transmit a clock pulse (see section 3 paragraph 4 of this Office action) between the delay sub-block (21, 23, and 25) and the correction block (3, 5, 7, 9 and 27).

With respect to claim 7, the resulting combination above produces a circuit, further comprising a node (at node Y) to transmit the conditioned clock pulse between the correction block (3, 5, 7, 9 and 27), the clock shuttle (p-type FETs of 11) and clock pulse inverter (13).

With respect to claim 8, the resulting combination above produces a circuit further comprising a leak detector (3) calculating a voltage potential between two digital devices.

With respect to claim 9, the resulting combination above produces a circuit wherein an uncorrected clock pulse bypasses (via n-type gates of 11 and wire between 11 and 13) the correction block (3, 5, 7, 9 and 27) and the clock shuttle (p-type FETs of 11) for delivery through the clock pulse output inverter (13).

With respect to claim 20, the resulting combination above produces a circuit comprising: a means for determining undesirable clock pulse width (3); a means (21, 23 and 25) for forwarding undesired clock pulses to a correction block (3, 5, 7, 9 and 27); a means (n-type FETs of element 11 and wire between 11 and 13), for desired clock pulses to bypass the pulse width correction and go directly to the device output; and a means (p-type FETs of 11) for incrementing a sequential delay for cascading a series of delay sub-blocks (21, 23 and 25).

With respect to claim 21, the resulting combination above produces a circuit

comprising: a means for determining undesirable clock pulse width (3); a means (21, 23 and 25) for forwarding undesired clock pulses to a correction block (5, 7, 9 and 27); a means (n-type FETs of element 11 and wire between 11 and 13) for bypassing the correction block (3, 5, 7, 9 and 27) sending desired clock pulses directly to the device output; and a means (p-type FETs of 11) for incrementing a sequential delay for cascading a series of delay sub-blocks (21, 23 and 25).

Allowable Subject Matter

5. Claims 10-19 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 10-19, the prior art of record fails to disclose or suggest a method for performing a plurality of clock pulse widths limiting in clock pulse, comprising disconnecting and resetting individual delay sub-locks as recited.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KEA
3/30/2006

Quan Tra
Primary Examiner